REMARKS

Claims 1-7, 9, 10 and 13-22 are pending. Claims 8, 11 and 12 are canceled. Claim 1 has been amended to conform the claim structure to standard U.S. claim format. No change in claim scope is intended and no new matter has been introduced.

The Examiner is thanked for considering the references listed on the IDS filed on November 17, 2008.

The Examiner rejected claims 13, 14, 16 and 18-22 under 35 USC Section 102(b) as anticipated by U.S. Patent Publication No. 2002/0055979 by Koch. The Examiner rejected claims 1-7, 9, 10, 15 and 17 under 35 U.S.C. Section 103(a) as obvious over Koch in view of U.S. Patent No. 6,775,717 issued to Tang. The Examiner's rejections are respectfully traversed.

With regard to claims 1-7, 9 and 10, independent claim 1 recites, "the first programmable unit and the second programmable unit each comprises: a direct access unit core; a first external direct memory access channel interface on the first clock; and a second external direct memory access channel interface on the second clock," and claims 2-7, 9 and 10 depend from claim 1. The Examiner points to access unit 51, DMA 41, interface 42, paragraphs 45, 48, 51 and 56 and Figure 4 of Koch as teaching programming elements for a programmable unit. The cited portions of Koch do not disclose two programmable units each of which has two external direct memory access channel interfaces, each on one of two clocks. The Examiner contends that two external DMA channels is taught by Tang. The Examiner admits that the combination of Koch and Tang does not disclose two programmable units each of which has two direct memory access channels interfaces one on each of two clocks. The Examiner contends it would have been obvious to make this additional modification after combining Koch and Tang, without citing an additional reference. Tang is directed to an arbitration system for a system with a common bus clock. Tang teaches arbitration and reduction in latency between completion of a first data transfer of a first DMA channel interface and the set up of a second data transfer of a second DMA channel interface on the same bus and the same clock. The motivation to which the Examiner points for making the additional modification is reducing the latency time between DMA transfers. This would seem to motivate, if anything, adding a second direct memory access channel interface on a same clock, rather than motivating a second direct memory access

channel interface on a different clock. Accordingly, it is respectfully submitted that claims 1-7, 9 and 10 are not rendered obvious by Koch, alone or in combination with Tang, because the combination of Koch with Tang does not teach, disclose or motivate "the first programmable unit and the second programmable unit each comprises: a direct access unit core; a first external direct memory access channel interface on the first clock; and a second external direct memory access channel interface on the second clock," as recited. It is noted that the Examiner commented that the previous amendment was attacking the references separately. It is respectfully submitted that the previous and current amendments argue that the suggested combination of references fails to disclose every element recited in the claims, which is required to establish a prima facie case of obviousness.

Independent claim 13 recites, "a first bi-directional channel to couple the second processor to the first shareable unit via the first and second busses, the first bi-directional channel configured to decouple the clock domain of the second processor from the clock domain of the first shareable unit, the first bi-directional channel also coupled through a first programming interface to the second processor; and a second bi-directional channel to couple the first processor to the second shareable unit via the first and second busses, the second bi-directional channel configured to decouple the clock domain of the first processor from the clock domain of the second shareable unit, the second bi-directional channel also coupled through a second programming interface to the first processor, the second bi-directional channel being simultaneously operable with the first bi-directional channel between the first and second bus." Independent claim 20 recites "coupling a first processor in the first processor environment to a first shareable unit in the second processor environment over a first programmable bi-directional channel of the plurality of programmable bi-directional channels; and coupling a second processor in the second processor environment to a second shareable unit in the first processor environment over a second programmable bi-directional channel of the plurality of programmable bi-directional channels." Claims 14, 16, 18 and 19 depend from claim 13 and claims 21 and 22 depend from claim 20. Koch, alone or in combination with Tang, does not teach first and second bi-directional channels, the first bi-directional channel being coupled through a first programming interface to a second processor and the second bi-directional

channel being coupled through a second programming in interface to a first processor. Accordingly, claims 13, 14, 16 and 18-22 are not anticipated by Koch.

Claim 15 depends from claim 13 and recites, "the second bi-directional channel comprises: a second external channel of the first DMA unit to operate on the first processor clock; a second external channel of the second DMA unit to operate on the second processor clock." Claim 17 depends from claim 13 and recites, "a second external channel of the first DMA unit to operate on the first processor clock; a second external channel on the second DMA unit to operate on the second processor clock." Thus, claims 15 and 17 are not anticipated or rendered obvious by Koch, alone or in combination with Tang, for reasons that will be apparent in view of the arguments presented above with respect to claim 1.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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